WHAT IS CLAIMED IS:

1. A liquid crystal display comprising:

a liquid crystal panel including a plurality of pixel rows, a plurality of data lines for transmitting data voltages to the pixel rows, a plurality of gate lines for transmitting gate signals to the pixel rows;

a signal controller for generating a control signal for controlling timing of the gate signals;

a data driver for providing the data voltages for the pixel rows through the data lines under control of the signal controller; and

a gate driver for providing the gate signals to the pixel rows in sequence through the gate lines based on the control signal of the signal controller,

wherein the pixel rows includes a plurality of pairs of first and second pixel rows adjacent to each other, sequentially arranged in a data voltage moving direction, and supplied with the data voltages having different polarities, the gate signals include first and second gate signals respectively applied to the first and the second pixel rows, and pulse widths of the second gate signals are increased by first modulation times.

2. The liquid crystal display of claim 1, wherein pulse widths of the first gate signals are decreased by second modulation times.

3. The liquid crystal display of claim 2, wherein the polarity of the data voltages are reversed every two pixel rows and the first modulation times are substantially equal to the respective second modulation times.

4. The liquid crystal display of claim 1, wherein the first modulation time for the second pixel row farther from inputs of the data voltages has a larger value.

5. The liquid crystal display of claim 4, wherein the first modulation time for a third pixel row among the second rows is determined by:

$A - B(I - I_{last})^P$ (p=1, 2, ...),

where I indicates a sequential index of the third pixel row, I_{last} indicates a sequential index of the last second pixel row, and A and B are values determined by characteristics of the liquid crystal panel.

6. The liquid crystal display of claim 5, wherein the values A and B are stored in a memory disposed at either inside or outside of the signal controller and the signal controller calculates the first modulation time based on the expression $A - B(I - I_{last})^P$.

7. The liquid crystal display of claim 4, wherein the pixel rows are classified into at least two groups, and the first modulation time for each group linearly increases along the data voltage moving direction.

8. The liquid crystal display of claim 7, wherein the first modulation times for the pixel rows at boundaries of the groups are stored in an internal or in an external memory of the signal controller.

9. The liquid crystal display of claim 1, wherein the signal controller provides a gate clock with a period increasing based on the first modulation time, and a pulse of each gate signal starts in synchronization with a rising edge of the gate clock and finishes at a next rising edge of the gate clock.

10. The liquid crystal display of claim 1, further comprising a delay circuit including a resistor and a capacitor connected in series between the signal controller and a reference voltage, the signal controller provides a first signal for the delay circuit and receives a second signal from the delay circuit, and the first modulation time is determined by a delay between the first signal and the second signal.

11. The liquid crystal display of claim 10, wherein the first modulation time for a pixel row is determined by a polynomial expression having the first modulation time for at least one pixel row as a coefficient.

12. The liquid crystal display of claim 11, wherein the first modulation time for the at least one pixel row is varied depending on the resistance of the resistor.